REMARKS

The Office Action mailed July 5, 2001, has been received and reviewed. Claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27, and 28 are currently pending in the application. Claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27, and 28 stand rejected. Applicant has amended claims 1, 3, 19, and 21, and respectfully requests reconsideration of the application as amended herein.

Objection to Title

The title of the invention was objected to as "not descriptive" and containing "method language." The title has been amended, as set forth above, to overcome the objection and more clearly describe the invention.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,955,781 to Joshi et al.

Claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27, and 28 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Joshi et al. (U.S. Patent No. 5,955,781). Applicant respectfully traverses this rejection, as hereinafter set forth.

Joshi et al. does not disclose a contact for a semiconductor device or a semiconductor device using contacts as presently claimed. Instead, the disclosure of Joshi et al. "describes a method and apparatus for the integration of diamond into VLSI circuit processing technology thereby using diamond as a heat sink to remove heat." *See, Joshi et al.* at col. 4, lines 64-67. Although Joshi et al. displays contacts (206) and interconnects (242) in its figures, Joshi et al. does not describe the contacts (206) or interconnects (242) sufficiently to anticipate the claims of the present invention.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention

must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicant submits that the local interconnect (242) structure of Joshi et al. is not a contact land as claimed in claims 1, 3, 4-6, 9, 10, 19, 21-24, 27, and 28. Instead, local interconnects (242) are similar to the source contact metallization 252 and drain contact metallization 254 as described in the present application with reference to the prior art. The local interconnects (242) may be used to form multilevel structures, but they are not contact lands for helping reduce problems associated with etch misalignments.

Furthermore, independent claim 1 is amended herein to recite "an individual contact land disposed atop said single contact plug and a portion of said first barrier layer." Joshi et al. does not disclose such a structure. Joshi et al. clearly states that "contacts 206 and local interconnects 242 to the devices are opened up into an oxide layer 244." In each of the figures of Joshi et al., local interconnect (242) is shown within oxide layer (244) and having a planar surface with the oxide layer (244). As amended, claim 1 recites the limitation that the individual contact land is disposed atop a portion of the first barrier layer, which is not described or shown by Joshi et al. Thus, Joshi et al. fails to anticipate amended claim 1.

Amended independent claim 19 is not anticipated by Joshi et al. for the same reasons that independent claim 1 is not anticipated.

Independent claim 3 is also amended to include the same limitation as claimed in claim 1. Joshi et al. does not show or describe a local interconnect (242) disposed atop a portion of the oxide layer (244) which is compared to the first barrier layer claimed in claim 3. Without an explicit, or implicit, description of an "individual [source or drain] contact land disposed atop each of said at least one [source or drain] contact plugs and a portion of said first barrier layer," Joshi et al. does not anticipate claim 3 under 35 U.S.C. § 102(e).

Amended independent claim 21 is not anticipated by Joshi et al. for the same reasons that independent claim 3 is not anticipated.

Claims 4 and 22 depend from allowable independent claims and are therefore also allowable over the present anticipation rejection. Furthermore, claims 4 and 22 recite "drain contact metallization" and "source contact metallization" that is not described by Joshi et al. If the interconnects (248) of Joshi et al. anticipate the upper source and drain contacts claimed in independent claims 3 and 21, as indicated in the Official Action, then the interconnects (248) cannot also anticipate a different structural limitation, in this case the source and drain contact metallization. The failure of Joshi et al. to describe the additional structural limitations as claimed in claims 4 and 22 precludes the present anticipation rejection.

Claims 5, 6, 9 and 10, and claims 23, 24, 27 and 28 depend from separate independent claims, respectively, but are independently allowable because Joshi et al. fails to describe each and every element of the claims in as complete detail as is contained in the claims. *See, Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). For instance, claims 5 and 23 recite the limitation "wherein said at least one source contact plug extends between at least two source regions." Similarly, claims 6 and 24 recite the limitation "wherein said at least one drain contact plug extends between at least two drain regions." The Official Action compares the contact (206) of Joshi et al. to the at least one source contact plug and the at least one drain contact plug of claims 5, 6, 23 and 24. However, nowhere in Joshi et al. is there any mention that the contact (206) may extend between more than one source or drain region. Without an explicit description of a source or drain contact (206) extending between "at least two [source or drain] regions," Joshi et al. does not anticipate claims 5, 6, 23 and 24.

Likewise, claims 9, 10, 27 and 28 include limitations not described by Joshi et al. First, Joshi et al. fails to describe contact lands recited in the claims, as previously discussed. Second, each of claims 9, 10, 27 and 28 involve upper source and drain contacts which are compared to the interconnects (248) illustrated in Joshi et al. However, Joshi et al. never describes an interconnect (248) extending between more than one contact land. Even if the local interconnects (242) anticipate the contact lands of the present invention, Joshi et al. fails to explicitly or implicitly describe "at least one upper [source or drain] contact [extending] between

at least two individual [source or drain] contact lands." This failure precludes an anticipation rejection of claims 9, 10, 27 and 28. *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Furthermore, claims 5, 6, 9 and 10, and claims 23, 24, 27 and 28 are not anticipated by Joshi et al. because the independent claims from which they depend are not anticipated by Joshi et al.

The Official Action indicates that the preambles to claims 3 and 21 are not given any weight because they recite an intended use of the device. The Nakamura et al. reference cited in the previous Official Action is cited as having an identical structure as the claimed invention. However, the present Official Action does not recite Nakamura et al. as an anticipatory reference. Applicant previously pointed out why Nakamura et al. is not an anticipatory reference and hereby incorporates those arguments with this paper. Claims 3 and 21 are in allowable form.

ENTRY OF AMENDMENTS

The amendments to claims 1, 3, 19, 21 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27, and 28 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully Submitted,

Devin R. Jensen
Registration Number 44,805
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
Telephone: (801) 532-1922

DRJ/ps:jb
Date: October 5, 2001
Enclosure: Version With Markings to Show Changes Made

N:\2269\3522\011005 - ROA - draft.wpd

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please replace the title at page 1 and the top of page 2 with the following:

ESD/EOS PROTECTION STRUCTURE FOR INTEGRATED CIRCUIT DEVICES [AND METHODS OF FABRICATING THE SAME]

IN THE CLAIMS:

1. (Four Times Amended) A contact for a semiconductor device, comprising:

a single contact plug extending through a first barrier layer, said single contact plug in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop said single contact plug and a portion of said first barrier layer, wherein said contact land is wider than said single contact plug and is substantially planar;

an upper contact extending through a second barrier layer, said second barrier layer disposed over said first barrier layer, to form an electrical contact with said individual contact land.

3. (Four Times Amended) A transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one drain region and said at least one source region on said at least one active area;

a first barrier layer substantially covering said at least one field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one source region on said semiconductor substrate;

an individual drain contact land disposed atop each of said at least one drain contact plugs and a portion of said first barrier layer, said individual drain contact land wider than said at least one drain contact plug and substantially planar;

an individual source contact land disposed atop each of said at least one source contact plugs and a portion of said first barrier layer, said individual source contact land wider than said at least one source contact plug and substantially planar;

a second barrier layer disposed over said first barrier layer, said individual drain contact land, and said individual source contact land;

at least one upper source contact extending through said second barrier layer, said at least one upper source contact is in electrical communication with at least one of said individual source contact lands; and

at least one upper drain contact extending through said second barrier layer, said at least one upper drain contact in electrical communication with at least one of said individual drain contact lands.

4. (Previously Amended) The transistor of claim 3, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

5. (Previously Twice Amended) The transistor of claim 3, wherein said at least one source contact plug extends between at least two source regions.

6. (Previously Twice Amended) The transistor of claim 3, wherein said at least one drain contact plug extends between at least two drain regions.

9. (Previously Three Times Amended) The transistor of claim 3, wherein said at least one upper source contact extends between at least two individual source contact lands.

10. (Previously Three Times Amended) The transistor of claim 3, wherein said at least one upper drain contact extends between at least two individual drain contact lands.

19. (Four Times Amended) A semiconductor device including at least one contact, comprising:

a single contact plug extending through a first barrier layer, said single contact plug in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop said single contact plug and a portion of said first barrier layer, said individual contact land wider than said single contact plug and substantially planar; and

an upper contact extending through a second barrier layer, said second barrier layer disposed over said first barrier layer, to form an electrical contact with said individual contact land.

21. (Four Times Amended) A semiconductor device including at least one transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer substantially covering said at least one thick field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one implanted drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one implanted source region on said semiconductor substrate;

an individual drain contact land disposed atop said at least one drain contact plug and a portion of said first barrier layer, said individual drain contact land wider than said at least one drain contact plug;

an individual source contact land disposed atop said at least one source contact plug and a portion of said first barrier layer, said individual source contact land is wider than said at least one source contact plug;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, said at least one upper source contact in electrical communication with at least one said individual source contact land; and

at least one upper drain contact extending through said second barrier layer, said at least one upper drain contact in electrical communication with at least one said individual drain contact land.

22. The semiconductor device of claim 21, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

23. (Previously Amended) The semiconductor device of claim 21, wherein said at least one source contact plug extends between at least two source regions.

24. (Previously Amended) The semiconductor device of claim 21, wherein said at least one drain contact plug extends between at least two drain regions.

27. (Previously Amended) The semiconductor device of claim 21, wherein said at least one upper source contact extends between at least two individual source contact lands.

28. (Previously Twice Amended) The semiconductor device of claim 21, wherein said at least one upper drain contact extends between at least two individual drain contact lands.